30.2 A 70GHz Manufacturable Complementary LC-VCO with 6.14GHz Tuning Range in 65nm SOI CMOS

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Realization of millimeter-wave (MMW) communication data link has been explored through VCO designs in CMOS technology [1-9]. While a higher VCO oscillation frequency has been pursued by driving VCO designs up to the technology limits, their manufacturability has been a concern. Due to increasing process variation in sub-100nm technologies, the VCO designs in digital microprocessor as an SoC require statistical design for functional yield, in addition to common VCO performance specifications. Because of technology scaling and process variation, a frequency tuning range (FTR) coverage that statistically overcomes the variation is necessary for the manufacturing of MMW VCO in SoC.

The proposed VCO circuit is implemented on a 65nm SOI CMOS process that provides up to 330 and 210GHz f_T for NFET and PFET. Compared with bulk CMOS, FET in SOI technology has lower parasitic diffusion-to-substrate capacitance due to buried oxide layer isolation. This is advantageous to a SOI-based LC VCO design, since less FET parasitic capacitance provides more tunable relative capacitance range to varactor. It also enhances maximum attainable center oscillation frequency (f_0). To achieve wide FTR, a complementary design is used, whose schematic diagram is depicted in Fig. 30.2.1. It has a symmetric complementary negative g_m (NFET for M1, M2, and PFET for M3, M4), an LC tank, composed of C-shape inductor and accumulation-mode MOS varactor (AMOS). Common-drain buffers (M5 and M6) are integrated for reduced parasitic capacitance coupling to oscillation nodes (V_A and V_B). The complementary VCO has V_A and V_B biasing at about half of V_{DD}. This biasing provides maximum capacitance tuning range to the AMOS, which is controlled by V_{CTRL} from 0 to V_{DD}. The wide FTR from the described AMOS biasing is achieved with PFET use, instead of inductive loads. PFET contributes additional capacitance, and it lowers maximum attainable oscillation frequency. But the complementary design consumes less current than cross-coupled NFET with inductive loads design, and it has better phase-noise property. Both NFET and PFET gate pitches are stretched to enhance carrier mobility and to reduce parasitic capacitance. The buffer output is collected by a grounded bias tee, as described in the Fig 30.2.1. A V-band mixer converts RF output to IF with 14th harmonic of LO signal. The mixer conversion loss is about 35 to 40dB, and there is at least 15dB power loss in the probe, cable, and adapter. The VCO output power coming into mixer RF input is insufficient for mixer operation and the spectrum analyzer LO signal is amplified by an LNA to turn the mixer on.

A 70GHz VCO design has many challenges. Due to complexity, it is desirable to use lumped element-based circuit design methodology. Active device models are extrapolated to V-band from lower frequency-based models. The inductor is calculated as a micro strip line, whose model is shown in Fig. 30.2.2. A 1.2μm-thick top copper layer is used to maximize Q and to reduce parasitic capacitance. RF skin effect at the target frequency is taken into account for realistic resistance estimation. The inductor is optimized for Q-factor, parasitic capacitance, inductance, and oscillation frequency, as depicted in the left bottom plot. Varactor is optimized for the highest Q-factor. The total capacitance and number of fingers are fixed, and the AMOS gate length and width are changed for the fixed capacitor and finger values. In the bottom right plot of Fig. 30.2.2, the varactor Q with gate-length sweep is calculated in the solid line. The corresponding gate width is obtained in the dotted line. An LC tank used in the VCO is analyzed with a network analyzer as plotted in the upper right graph. An estimated Q-factor is about 8.5 with a de-embedding. Instead of directly characterizing the inductor and varactor separately, which is challenging due to their small size and values, the LC tank measurement is used as an alternative characterization method. All designs are conducted with standard digital microprocessor technology and models.

The VCO uses V_{DD}=1.2V and the output spectrum is captured at Fig. 30.2.3. The peak frequency is ~73.47GHz with -35dBm output power, and the marker phase-noise measurement is better than -92.9dBc/Hz at 10MHz offset. The phase-noise measurement is limited by signal power and thermal noise floor. The oscillation frequency of the same circuit with V_{CTRL} sweep is shown in the right plot. The circuit operates from the lowest tunable frequency f_L=66.8 to the highest tunable f_H=73.5GHz. The center frequency f_0, average of f_L and f_H, is 70.1GHz. The FTR of the VCO is 6.68GHz, or 9.05% of f_0. In the plot, the maximum VCO gain (K_v) is 9.09GHz/V at f_0, and the minimum K_v is 2.37GHz/V at f_L. The VCO phase noise is not directly measurable due to weak signal and setup insertion loss. As shown in the test setup diagram in Fig. 30.2.4, the VCO output is divided by 2 thru an on-chip divider, and phase noise is measured with a spectrum analyzer. The VCO oscillates at 63.86GHz, and the divided output frequency is 31.93GHz. Measured phase noise is -112.14dBc/Hz at 10MHz offset. The estimated VCO phase noise is -106.14dBc/Hz at 10MHz offset, when 6dB improvement from frequency division is compensated.

The frequency tuning tests are performed on 57 sites in a 300mm wafer, and VCO properties are statistically analyzed in Fig. 30.2.5. Average VCO current is 4.48mA with V_{DD}=1.2V, or 5.37mW in the VCO core, excluding buffer current, whose average is ~3.96mA at 1.2V supply. With these statistics, the manufacturability of VCO can be evaluated. In this wafer, the probability that a circuit fails to pass 67.9GHz oscillation-frequency specification is almost zero, considering 67.9GHz f_0, 0.79GHz f_0 standard deviation, and 6.14GHz average FTR. The relation between FTR and functional yield is visualized in the bottom plot. The lowest and highest tunable frequency f_L and f_H from 57 sites on the wafer are sorted by descending FTR. The common FTR for all circuits is defined as a difference between minimum f_H and maximum f_L, and it is 66.9 to 69.9GHz as marked in the plot. All VCOs pass designated oscillation-frequency specification in the common FTR. In case of the 70GHz target oscillation frequency, 3 circuits fail the functional requirement out of 57 as crossed in the figure. The VCO functional yield in this wafer is 94.7%.

In light of up to 10% changes of 3σ active and passive device variations in CMOS technologies, it is essential for a VCO to have a wide FTR to be manufactured as an SoC. Figure 30.2.6 shows state-of-the-art CMOS VCOs with >50GHz oscillation frequency. The proposed complementary VCO oscillates at 70GHz with 9.05%, or 6.14GHz FTR, and functional yield of 94.7% on a 65nm SOI 300mm wafer. A die mircrograph is shown in Fig. 30.2.7. The total VCO circuit area, including VCO core, buffer, and inductor, except pads, is 60×45μm^2. The complementary MOS design saves silicon estate by using PFETs in place of inductive loads, and it lowers power consumption to 5.4mW with -106.14dBc/Hz phase noise at 10MHz offset.

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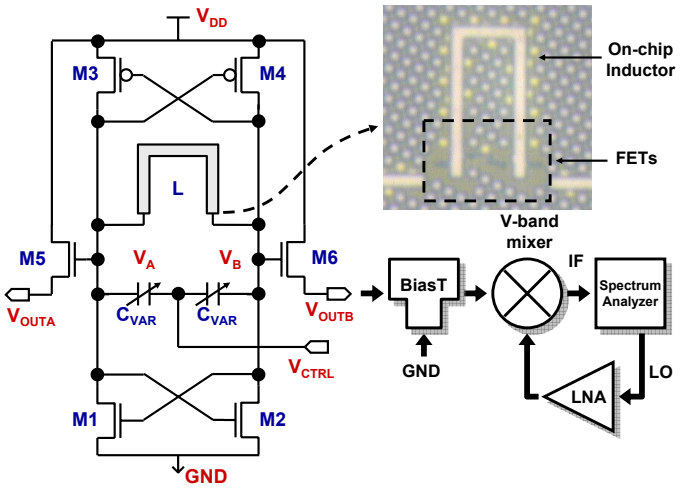

Figure 30.2.1: Complementary VCO schematic and test setup.

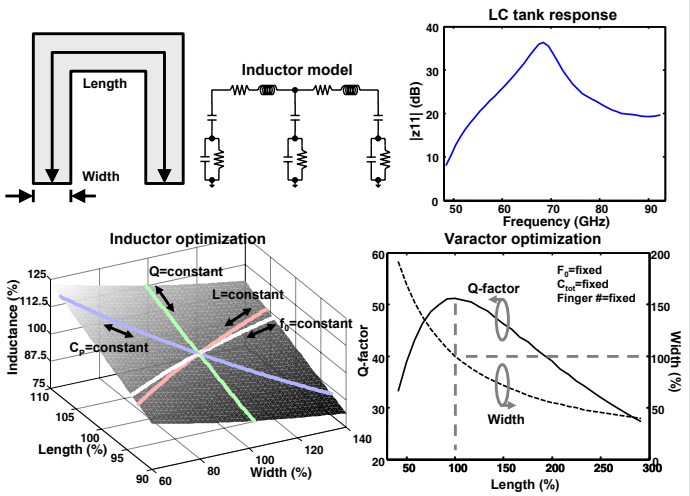

Figure 30.2.2: Inductor and varactor design.

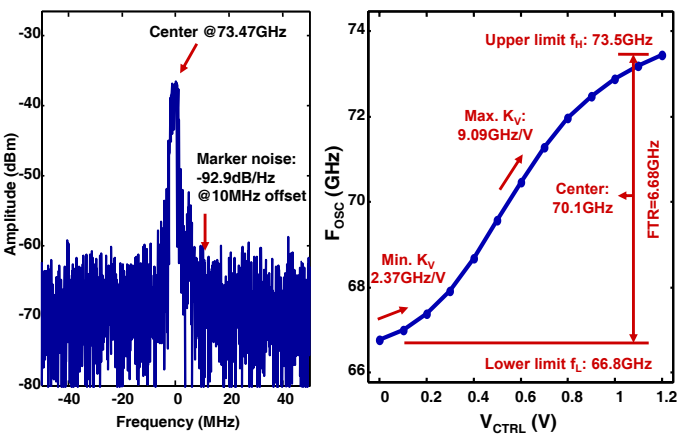

Figure 30.2.3: VCO output spectrum and frequency tuning range.

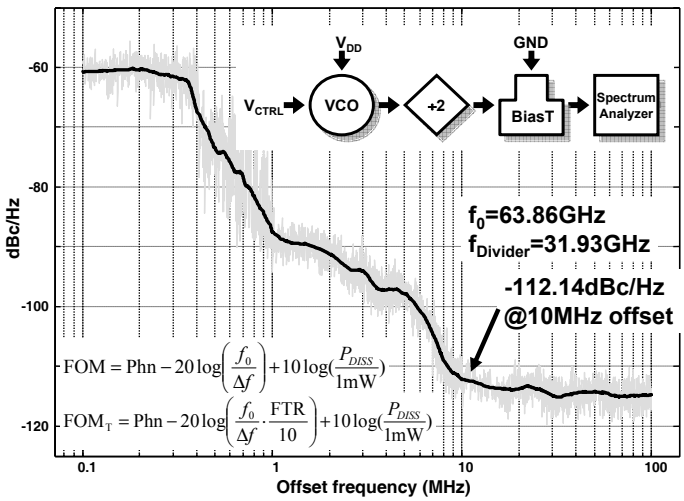

Figure 30.2.4: Phase noise measurement and test set-up.

	Average	Standard deviation	Normalized deviation (%)	Max.	Min.
Upper limit f_H (GHz)	71.0	0.82	1.15	73.5	69.9
Lower limit f_L (GHz)	64.8	0.76	1.18	66.9	63.8
Center frequency f_0 (GHz)	67.9	0.79	1.16	70.1	66.9
FTR (GHz)	6.14	0.13	2.11	6.68	5.91
FTR (%)	9.05	0.17	1.90	9.53	8.72
Full range VCO gain (GHz/V)	5.11	0.11	2.11	5.57	4.93
Max VCO gain (GHz/V)	7.96	0.43	5.36	9.38	7.25
Min VCO gain (GHz/V)	1.72	0.43	25.0	2.37	0.11
I_{VDD} (mA) @ V_{CTRL}=0	4.48	0.51	11.4	5.15	3.59

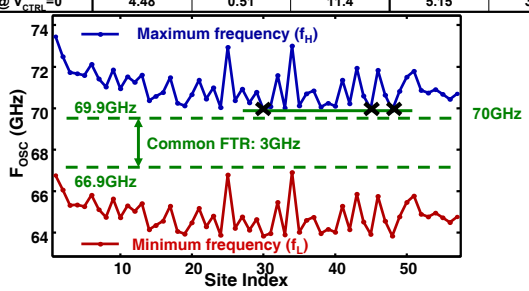

Figure 30.2.5: VCO statistics from a 300mm wafer.

VCO [Ref]	FO (GHz)	FTR (%)	Phase Noise (dBc/Hz)	P_{DISS} (mW)	FOM (dBc/Hz)	FOM_T (dBc/Hz)	Technology
M. Tiebout [1]	51.2	1.39%	-85 @1MHz	1.0	-179.19	-162.03	0.12µm CMOS
F. Ellinger [2]	56.5	14.70%	-92 @1MHz	21.0	-173.81	-177.16	90nm SOI
C. Cao [3]	56.5	10.27%	-108 @10MHz	9.8	-173.13	-173.36	0.13µm CMOS
R.-C. Liu [4]	64.3	7.00%	-85 @1MHz	118.8	-160.41	-157.32	0.25µm CMOS
C. Cao [5]	89.7	2.68%	-106 @10MHz	15.8	-173.08	-161.63	0.13µm CMOS
C. Cao [3]	98.5	2.54%	-102.7 @10MHz	7.0	-174.12	-162.21	0.13µm CMOS
L. M. Franca-Neto [6]	103.9	1.92%	-94 @10MHz	180.0	-151.78	-137.47	90nm CMOS
C. Cao [3]	105.2	0.19%	-97.5 @10MHz	7.2	-169.37	-134.95	0.13µm CMOS
P.-C. Huang [7]	114.0	2.11%	-107.6 @10MHz	8.4	-179.50	-165.96	0.13µm CMOS
P.-C. Huang [8]	130.9	1.68%	-108.4 @10MHz	20.0	-177.73	-162.24	90nm CMOS
C. Cao [9]	192.1	0.68%	-100 @10MHz	16.5	-173.49	-150.10	0.13µm CMOS
This work	**70.2**	**9.55%**	**-106.14 @10MHz**	**5.4**	**-175.76**	**-175.36**	**65nm SOI**

Figure 30.2.6: State-of-the-art VCOs over 50GHz.

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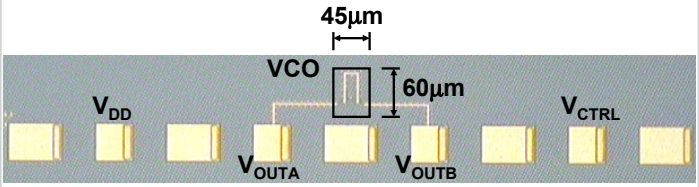

Figure 30.2.7: VCO die micrograph.

